**Sveučilište J.J. Strossmayera u Osijeku**
**Odjel za matematiku**

# GRAĐA RAČUNALA

(predavanja u ak. god. 2005./2006.)

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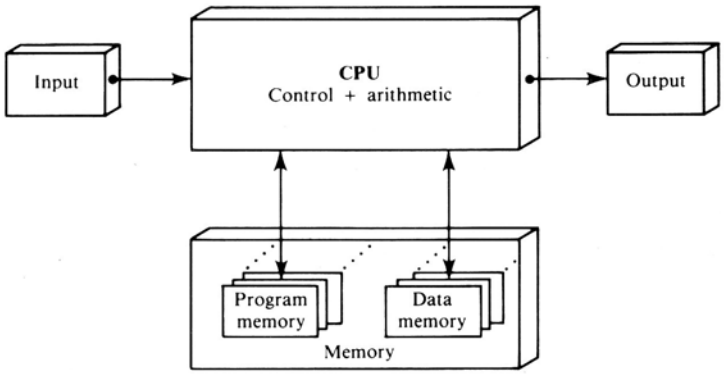
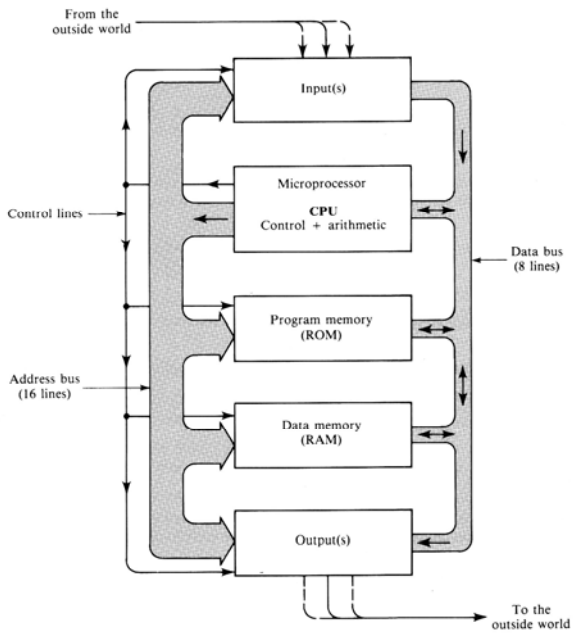
Osijek, 2006.



UVOD U RAČUNALA




Opća organizacija računala




Uobičajena organizacija mikroračunala

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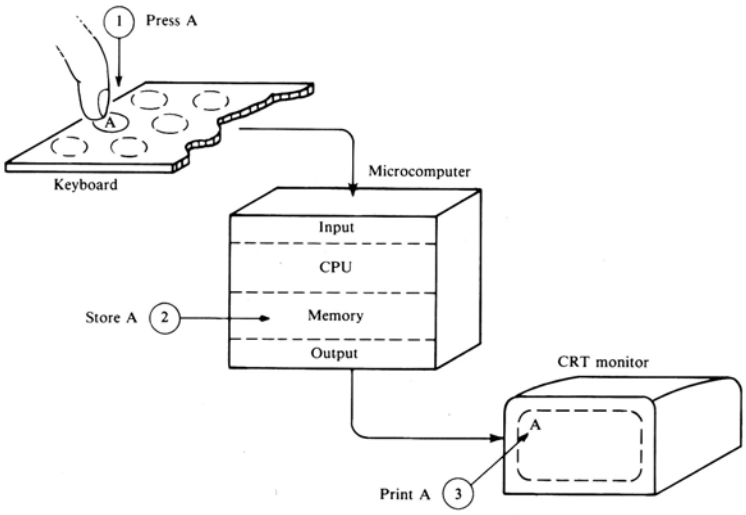
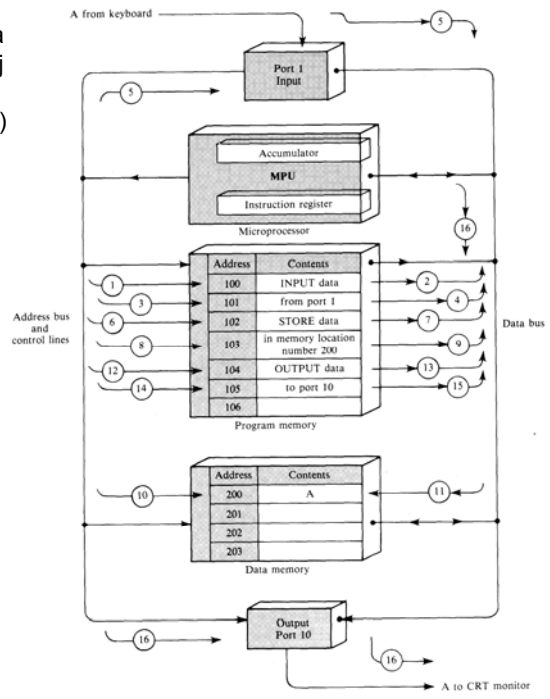



Uobičajeni način rada računala

4

Koraci izvođenja programa Smještenog u programskoj Memoriji
(dohvati - dekodiraj - izvrši)




## BROJEVI, KODOVI I ARITMETIKA

Decimalni i binarni ekvivalenti

| Powers of 10 | $10^3$ | $10^2$ | $10^1$ | $10^0$ |
|---|---|---|---|---|
| Place value | 1000s | 100s | 10s | 1s |
| Decimal | **1** | **3** | **2** | **7** |
| Decimal | 1000 + | 300 + | 20 + | 7 = 1327 |

(*a*) Place values in a decimal number

| Powers of 2 | $2^3$ | $2^2$ | $2^1$ | $2^0$ |
|---|---|---|---|---|
| Place value | 8s | 4s | 2s | 1s |
| Binary | **1** | **0** | **0** | **1** |
| Decimal | 8 + | 0 + | 0 + | 1 = 9 |

MSB … LSB

(*b*) Place values in a binary number

| Decimal | | Binary | | | | Decimal | | Binary | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 10s | 1s | 8s | 4s | 2s | 1s | 10s | 1s | 8s | 4s | 2s | 1s |
| | 0 | | | | 0 | | 8 | 1 | 0 | 0 | 0 |
| | 1 | | | | 1 | | 9 | 1 | 0 | 0 | 1 |
| | 2 | | | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 |
| | 3 | | | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 |
| | 4 | | 1 | 0 | 0 | 1 | 2 | 1 | 1 | 0 | 0 |
| | 5 | | 1 | 0 | 1 | 1 | 3 | 1 | 1 | 0 | 1 |
| | 6 | | 1 | 1 | 0 | 1 | 4 | 1 | 1 | 1 | 0 |
| | 7 | | 1 | 1 | 1 | 1 | 5 | 1 | 1 | 1 | 1 |

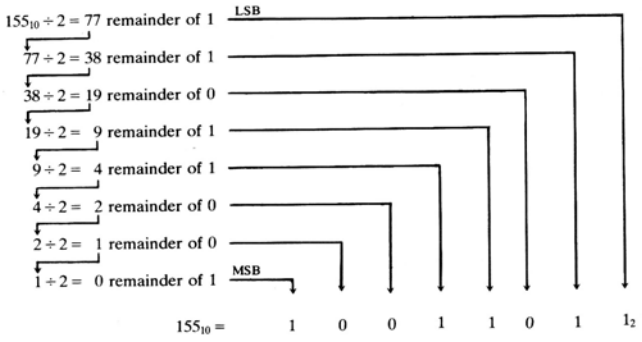
| Powers of 2 | $2^7$ | $2^6$ | $2^5$ | $2^4$ | $2^3$ | $2^2$ | $2^1$ | $2^0$ |
|---|---|---|---|---|---|---|---|---|
| Place value | 128s | 64s | 32s | 16s | 8s | 4s | 2s | 1s |
| Binary | **1** | **0** | **1** | **1** | **0** | **1** | **1** | **0** |
| Decimal | 128 | + | 32 | + 16 | + | 4 | + 2 | = 182 |

(*a*) Binary-to-decimal conversion

$10110110_2 = 182_{10}$

(*b*) Subscripts designate the base of the number

Potencije broja 2

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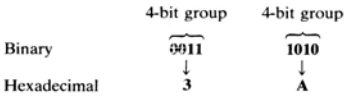
Primjer pretvorbe DEC -> BIN

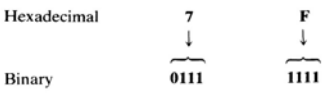
DEC, HEX i BIN sustavi

| Decimal | Hexadecimal | Binary 8s | 4s | 2s | 1s |
|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 1 | 0 | 0 | 0 | 1 |
| 2 | 2 | 0 | 0 | 1 | 0 |
| 3 | 3 | 0 | 0 | 1 | 1 |
| 4 | 4 | 0 | 1 | 0 | 0 |
| 5 | 5 | 0 | 1 | 0 | 1 |
| 6 | 6 | 0 | 1 | 1 | 0 |
| 7 | 7 | 0 | 1 | 1 | 1 |
| 8 | 8 | 1 | 0 | 0 | 0 |
| 9 | 9 | 1 | 0 | 0 | 1 |
| 10 | A | 1 | 0 | 1 | 0 |
| 11 | B | 1 | 0 | 1 | 1 |
| 12 | C | 1 | 1 | 0 | 0 |
| 13 | D | 1 | 1 | 0 | 1 |
| 14 | E | 1 | 1 | 1 | 0 |
| 15 | F | 1 | 1 | 1 | 1 |

Primjeri pretvorbe




(*a*) Binary-to-hexadecimal conversion




(*b*) Hexadecimal-to-binary conversion

8

| Powers of 16 | $16^3$ | $16^2$ | $16^1$ | $16^0$ |
|---|---|---|---|---|
| Place value | 4096s | 256s | 16s | 1s |

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| Hexadecimal | **2** | | **C** | | **6** | **E** | |
| | ↓ | | ↓ | | ↓ | ↓ | |
| | 4096 | | 256 | | 16 | 1 | |
| | ×2 | | ×12 | | ×6 | ×14 | |
| Decimal | 8192 | + | 3072 | + | 96 | + 14 | = $11{,}374_{10}$ |

(*a*) Hexadecimal-to-decimal conversion

$15{,}797_{10} \div 16 = 987$ remainder of $5_{10} = 5_{16}$ LSD

$987 \div 16 = 61$ remainder of $11_{10} = B_{16}$

$61 \div 16 = 3$ remainder of $13_{10} = D_{16}$

$3 \div 16 = 0$ remainder of $3_{10} = 3_{16}$ MSD

$15{,}797_{10} =$ 3 D B $5_{16}$

(*b*) Decimal-to-hexadecimal conversion

Primjeri pretvorbe



| Decimal | BCD 8s | 4s | 2s | 1s |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 0 | 1 |
| 2 | 0 | 0 | 1 | 0 |
| 3 | 0 | 0 | 1 | 1 |
| 4 | 0 | 1 | 0 | 0 |
| 5 | 0 | 1 | 0 | 1 |
| 6 | 0 | 1 | 1 | 0 |
| 7 | 0 | 1 | 1 | 1 |
| 8 | 1 | 0 | 0 | 0 |
| 9 | 1 | 0 | 0 | 1 |

(*a*) The 8421 BCD code

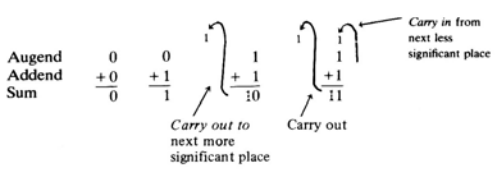
| | | | | |
|---|---|---|---|---|
| Decimal | 3 | 6 | 9 | 1 |
| | ↓ | ↓ | ↓ | ↓ |
| BCD | 0011 | 0110 | 1001 | 0001 |

(*b*) Decimal-to-BCD conversion

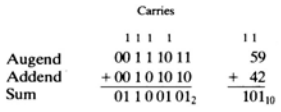
| | | | | |
|---|---|---|---|---|
| BCD | 1000 | 0000 | 0111 | 0010 |
| | ↓ | ↓ | ↓ | ↓ |
| Decimal | 8 | 0 | 7 | 2 |

(*c*) BCD-to-decimal conversion

8421 kod i primjeri pretvorbe

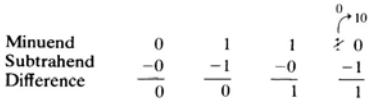



(a) Rules for binary addition

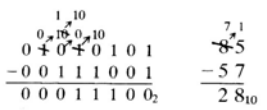



(b) Binary addition problem

Binarno zbrajanje



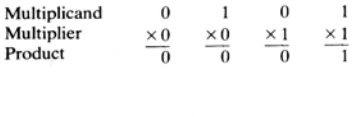

(a) Rules for binary subtraction



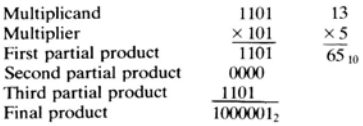
(b) Binary subtraction problem

Binarno oduzimanje



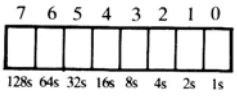



(a) Rules for binary multiplication

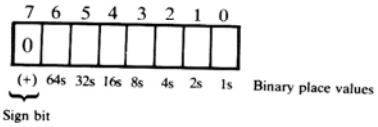



(b) Binary multiplication problem

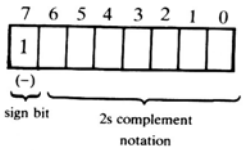
Binarno množenje




(a) Labeling storage locations in an 8-bit register




(b) Positive numbers identified by a 0 in the sign bit location in the register




(c) Negative numbers identified by a 1 in the sign bit location in the register

Brojevi s predznakom

Brojevi s predznakom
i njihovi binarni ekvivalenti

| Decimal | Representation of signed numbers | |
|---|---|---|
| +127 | 0111 1111 | Positive numbers represented the same as in straight binary |
| ⋮ | ⋮ | |
| +8 | 0000 1000 | |
| +7 | 0000 0111 | |
| +6 | 0000 0110 | |
| +5 | 0000 0101 | |
| +4 | 0000 0100 | |
| +3 | 0000 0011 | |
| +2 | 0000 0010 | |
| +1 | 0000 0001 | |
| +0 | 0000 0000 | |
| −1 | 1111 1111 | Negative numbers represented in 2s complement form |
| −2 | 1111 1110 | |
| −3 | 1111 1101 | |
| −4 | 1111 1100 | |
| −5 | 1111 1011 | |
| −6 | 1111 1010 | |
| −7 | 1111 1001 | |
| −8 | 1111 1000 | |
| ⋮ | ⋮ | |
| −128 | 1000 0000 | |

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| | | |
|---|---|---|
| Decimal | 9 | Step 1: Write decimal |
| | ↓ | Step 2: Convert to binary |
| Binary | 00001001 | |
| | ↓ | Step 3: Complement each bit |
| 1s complement | 11110110 | |
| | + 1 | Step 4: Add +1 |
| 2s complement | 11110111 = −9 | |

(*a*) Forming the 2s complement of a negative number

| | | |
|---|---|---|
| 2s complement | 11110000 | Step 1: Write 2s complement |
| | ↓ | Step 2: Complement each bit |
| 1s complement | 00001111 | |
| | + 1 | Step 3: Add +1 |
| Binary | 00010000 = 16 | |

(*b*) Finding the decimal equivalent for a 2s complement number

Pronalaženje decimalnog ekvivalenta za dvojni komplement broja 14

| | | |
|---|---|---|
| Augend | (+5) | 00000101 |
| Addend | +(+3) | +00000011 |
| Sum | (+8) | 00001000 |

(*a*) 2s complement addition problem

| | | |
|---|---|---|
| Augend | (+7) | 00000111 |
| Addend | +(−3) | +11111101 |
| Sum | (+4) | (1)00000100 |

Discard overflow

(*b*) 2s complement addition problem

| | | |
|---|---|---|
| Augend | (+3) | 00000011 |
| Addend | +(−8) | +11111000 |
| Sum | (−5) | 11111011 |

(*c*) 2s complement addition problem

| | | |
|---|---|---|
| Augend | (−2) | 11111110 |
| Addend | +(−5) | +11111011 |
| Sum | (−7) | (1)11111001 |

Discard overflow

(*d*) 2s complement addition problem

Aritmetika dvojnog komplementa - zbrajanje

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| | | | |
|---|---|---|---|
| Minuend | (+8) | | 00001000 |
| Subtrahend | −(+5) = 00000101 | Convert to 2s complement → | +11111011 |
| Difference | (+3) | | (1)00000011 |

Discard overflow

(*a*) 2s complement subtraction problem using addition

| | | | |
|---|---|---|---|
| Minuend | (+2) | | 00000010 |
| Subtrahend | −(+6) = 00000110 | Convert to 2s complement → | +11111010 |
| Difference | (−4) | | 11111100 |

(*b*) 2s complement subtraction problem using addition

Aritmetika dvojnog komplementa – oduzimanje pomoću zbrajanja

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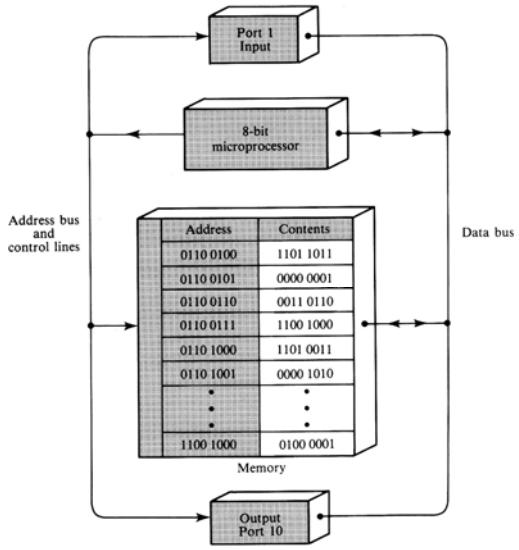


(*a*) Typical binary memory contents in a microcomputer

Sadržaj i interpretiranje sadržaja memorije

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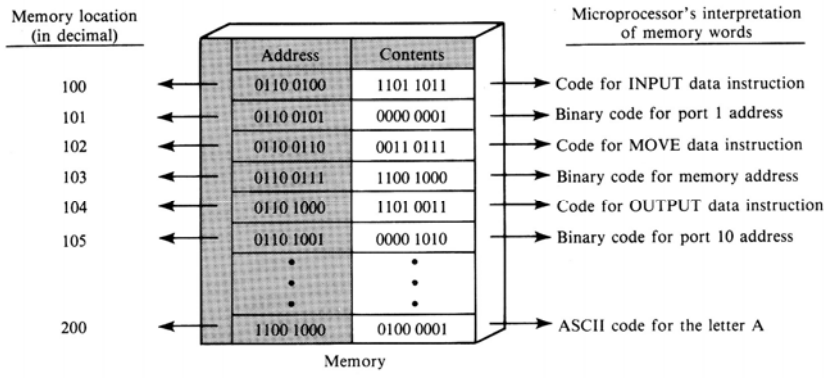


(*b*) The microprocessor's interpretations of the contents of memory

Sadržaj i interpretiranje sadržaja memorije

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Dio liste ASCII skupa znakova

| Character | ASCII | Character | ASCII |
|---|---|---|---|
| Space | 010 0000 | A | 100 0001 |
| ! | 010 0001 | B | 100 0010 |
| " | 010 0010 | C | 100 0011 |
| # | 010 0011 | D | 100 0100 |
| $ | 010 0100 | E | 100 0101 |
| % | 010 0101 | F | 100 0110 |
| & | 010 0110 | G | 100 0111 |
| ' | 010 0111 | H | 100 1000 |
| ( | 010 1000 | I | 100 1001 |
| ) | 010 1001 | J | 100 1010 |
| * | 010 1010 | K | 100 1011 |
| + | 010 1011 | L | 100 1100 |
| , | 010 1100 | M | 100 1101 |
| - | 010 1101 | N | 100 1110 |
| . | 010 1110 | O | 100 1111 |
| / | 010 1111 | P | 101 0000 |
| 0 | 011 0000 | Q | 101 0001 |
| 1 | 011 0001 | R | 101 0010 |
| 2 | 011 0010 | S | 101 0011 |
| 3 | 011 0011 | T | 101 0100 |
| 4 | 011 0100 | U | 101 0101 |
| 5 | 011 0101 | V | 101 0110 |
| 6 | 011 0110 | W | 101 0111 |
| 7 | 011 0111 | X | 101 1000 |
| 8 | 011 1000 | Y | 101 1001 |
| 9 | 011 1001 | Z | 101 1010 |

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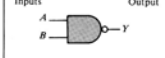
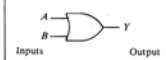
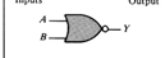
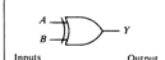
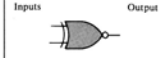
Logički sklopovi, funkcije i tablice stanja

OSNOVNI DIGITALNI SKLOPOVI

| Logic function | Logic gate symbol | Truth table | Boolean expression |
|---|---|---|---|
| Inverter |   | Input A / Output Ā: 0 → 1; 1 → 0 | $A = \bar{A}$ |
| AND |   | Inputs B A / Outputs AND NAND: 0 0 → 0 1; 0 1 → 0 1; 1 0 → 0 1; 1 1 → 1 0 | $A \cdot B = Y$ |
| NAND |   | | $\overline{A \cdot B} = Y$ |
| OR |   | Inputs B A / Outputs OR NOR: 0 0 → 0 1; 0 1 → 1 0; 1 0 → 1 0; 1 1 → 1 0 | $A + B = Y$ |
| NOR |   | | $\overline{A + B} = Y$ |
| Exclusive OR |   | Inputs B A / Outputs XOR XNOR: 0 0 → 0 1; 0 1 → 1 0; 1 0 → 1 0; 1 1 → 0 1 | $A \oplus B = Y$ |
| Exclusive NOR |  | | $\overline{A \oplus B} = Y$ |

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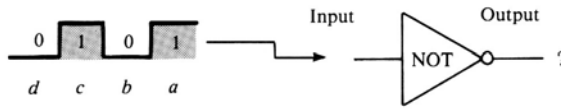
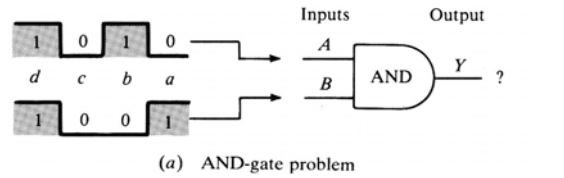
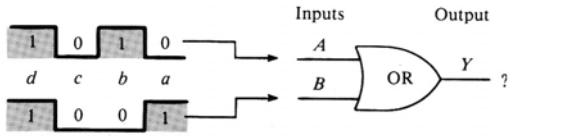
Problem invertora



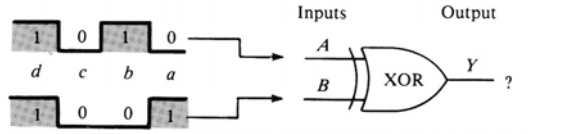

Problem EX-ILI vrata




(a) AND-gate problem




(b) OR-gate problem



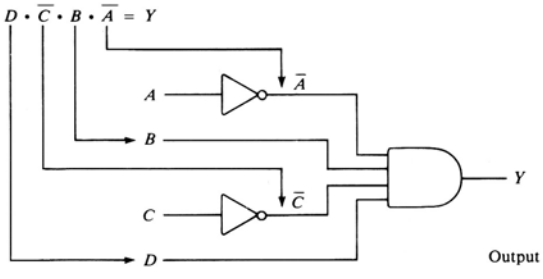

(c) XOR-gate problem

Kombinirani logički sklopovi

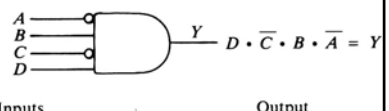
| Inputs | | | | Output | Inputs | | | | Output |
|---|---|---|---|---|---|---|---|---|---|
| D | C | B | A | Y | D | C | B | A | Y |
| 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 0 |
| 0 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 1 |
| 0 | 0 | 1 | 1 | 0 | 1 | 0 | 1 | 1 | 0 |
| 0 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 |
| 0 | 1 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 0 |
| 0 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 0 | 0 |
| 0 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 0 |

$\rightarrow D \cdot \bar{C} \cdot B \cdot \bar{A} = Y$

(a) Converting truth table to equivalent Boolean expression




(b) Converting Boolean expression to logic-symbol diagram

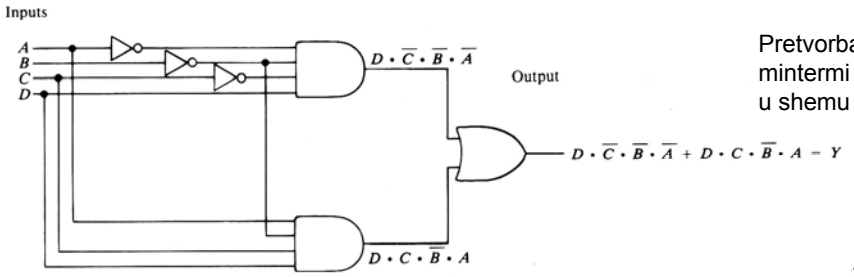



(c) Simplified logic-symbol diagram

| Inputs | | | | Output | Inputs | | | | Output | |
|---|---|---|---|---|---|---|---|---|---|---|
| $D$ | $C$ | $B$ | $A$ | $Y$ | $D$ | $C$ | $B$ | $A$ | $Y$ | |
| 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | $\rightarrow D \cdot \bar{C} \cdot \bar{B} \cdot \bar{A}$ |
| 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | |
| 0 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | |
| 0 | 0 | 1 | 1 | 0 | 1 | 0 | 1 | 1 | 0 | or |
| 0 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | |
| 0 | 1 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | $\rightarrow D \cdot C \cdot \bar{B} \cdot A$ |
| 0 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | |
| 0 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 0 | |

(*a*) Converting truth table to equivalent minterm Boolean expression

Pretvorba tablice stanja u minterme

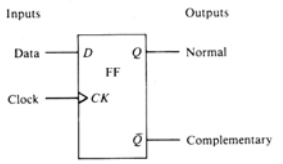



(*b*) Converting minterm Boolean expression into a logic-symbol diagram

Pretvorba mintermi u shemu sklopa



D bistabil



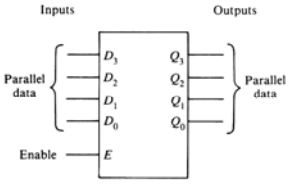

(*a*) Logic symbol for *D* flip-flop

| Mode of operation | Inputs | | Outputs | |
|---|---|---|---|---|
| | $D$ | $CK$ | $Q$ | $\bar{Q}$ |
| Set | 1 | ↑ | 1 | 0 |
| Reset | 0 | ↑ | 0 | 1 |
| Hold | X | No clock pulse | Same as before | |

0 = LOW
1 = HIGH
X = irrelevant
↑ = LOW-to-HIGH transition of the clock pulse

(*b*) Mode-truth table for *D* flip-flop

4-bitni bistabil



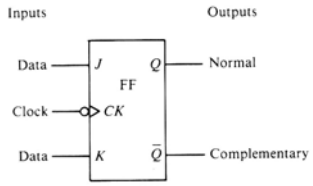

(*a*) Logic symbol for 4-bit transparent latch

| Mode of operation | Inputs | | Output |
|---|---|---|---|
| | $D$ | $E$ | $Q$ |
| Data enabled | 0 | 1 | 0 |
| | 1 | 1 | 1 |
| Data latched | X | 0 | Same as before |

0 = LOW
1 = HIGH
X = irrelevant

(*b*) Mode-truth table for latch

JK bistabil




(a) Logic symbol for *JK* flip-flop

| Mode of operation | Inputs | | | Outputs | |
|---|---|---|---|---|---|
| | *J* | *K* | *CK* | *Q* | $\bar{Q}$ |
| Toggle | 1 | 1 | ↓ | Opposite state | |
| Set | 1 | 0 | ↓ | 1 | 0 |
| Reset | 0 | 1 | ↓ | 0 | 1 |
| Hold | 0 | 0 | ↓ | No change | |

0 = LOW
1 = HIGH
↓ = HIGH-to-LOW transition of the clock pulse

(b) Mode-truth table for *JK* flip-flop

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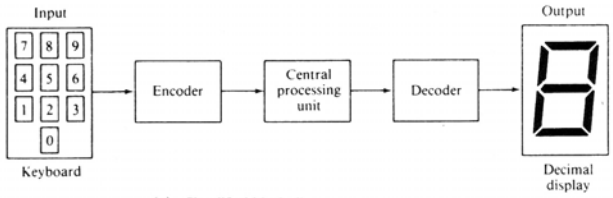
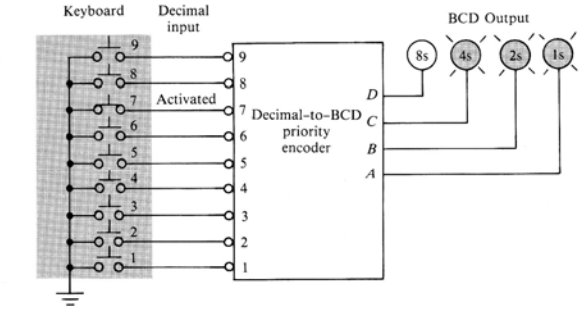
KODERI, DEKODERI I 7-SEGMENTNI POKAZIVAČI




(a) Simplified block diagram of calculator circuit




(b) Logic diagram of keyboard-encoder circuits

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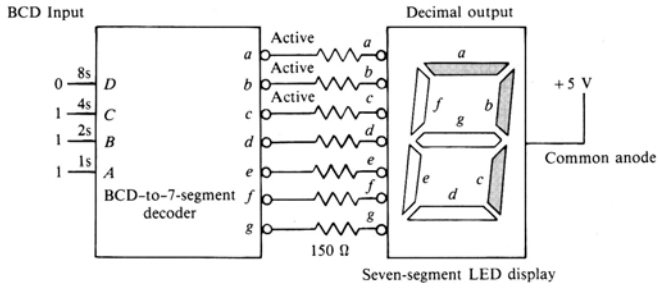


(c) Logic diagram of decoder-display circuits

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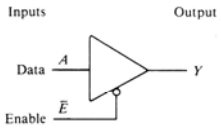
Three-state sabirnički spremnik

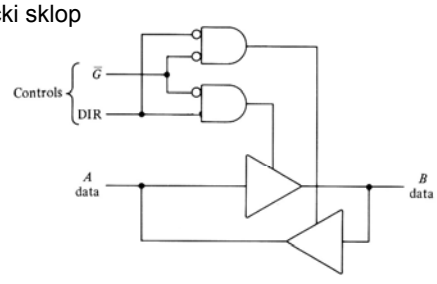



(a) Logic symbol for three-state bus buffer

| Mode of operation | Inputs $\bar{E}$ | Inputs $A$ | Output $Y$ |
|---|---|---|---|
| Enabled | 0 | 0 | 0 |
| | 0 | 1 | 1 |
| Disabled | 1 | 0 | High impedance (output voltage floats) |
| | 1 | 1 | |

(b) Mode-truth table for three-state bus buffer

Three-state sabirnički sklop

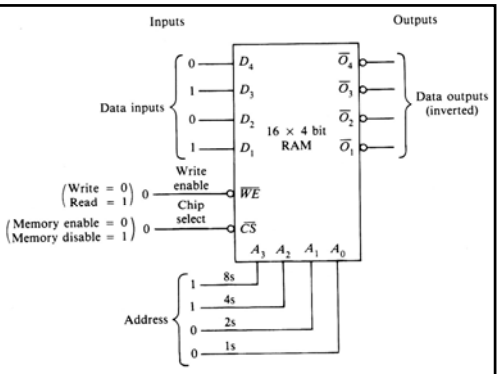



| Control inputs | | Operation |
|---|---|---|
| Enable $\bar{G}$ | Direction DIR | |
| L | L | $B$ data to $A$ bus |
| L | H | $A$ data to $B$ bus |
| H | X | Isolation (high $Z$) |

H = HIGH logic level
L = LOW logic level
X = irrelevent

(a) Logic diagram for three-state bus transceiver (b) Mode-truth table for three-state bus transceiver

| Address | Bit $D$ | Bit $C$ | Bit $B$ | Bit $A$ |
|---|---|---|---|---|
| Word 0 | | | | |
| Word 1 | | | | |
| Word 2 | | | | |
| Word 3 | | | | |
| Word 4 | | | | |
| Word 5 | | | | |
| Word 6 | | | | |
| Word 7 | | | | |
| Word 8 | | | | |
| Word 9 | | | | |
| Word 10 | | | | |
| Word 11 | | | | |
| Word 12 | 0 | 1 | 0 | 1 |
| Word 13 | | | | |
| Word 14 | | | | |
| Word 15 | | | | |




(*b*) Logic symbol for a 16×4 bit RAM

| Mode of operation | Control inputs | | Outputs |
|---|---|---|---|
| | $\overline{CS}$ | $\overline{WE}$ | $\overline{O}$ |
| Write | 0 | 0 | Logical 1 state |
| Read | 0 | 1 | Complement of data stored in memory |
| Hold | 1 | X | Logical 1 state |

X = irrelevant

(*c*) Mode-truth table for 64-bit RAM

16x4 RAM