Sveučilište J.J. Strossmayera u Osijeku
Odjel za matematiku

GRAĐA RAČUNALA

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Osijek, 2006.

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OSNOVE GRAĐE MIKRORAČUNALA

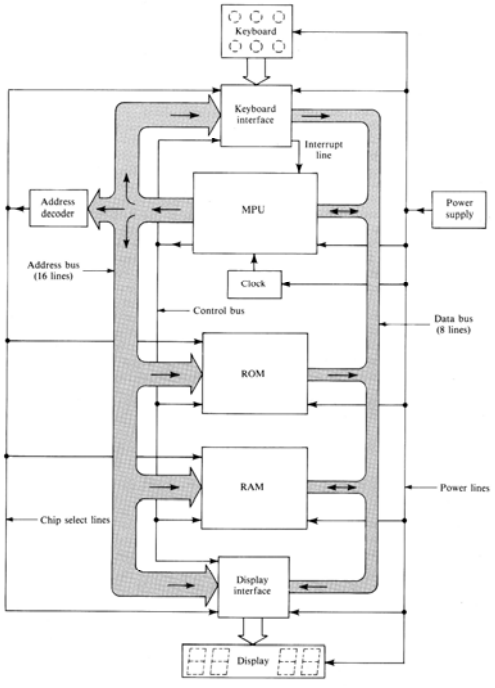
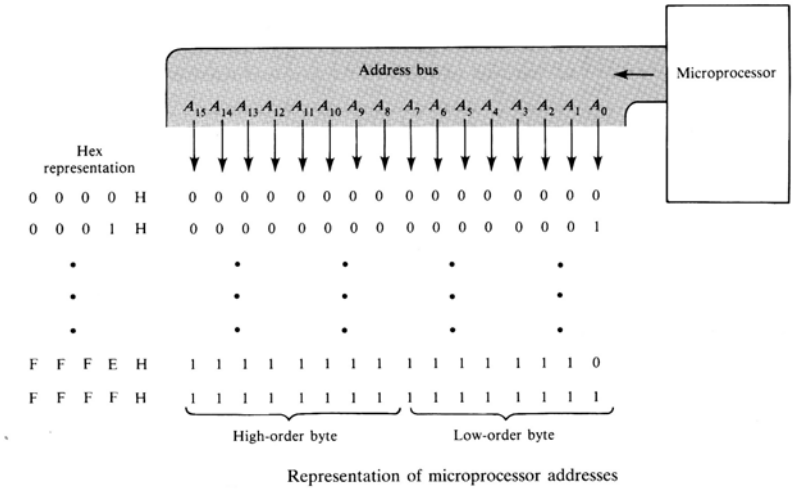


Fig. 4-1 Microcomputer architecture

Pojednostavljena organizacija memorije



Representation of microprocessor addresses

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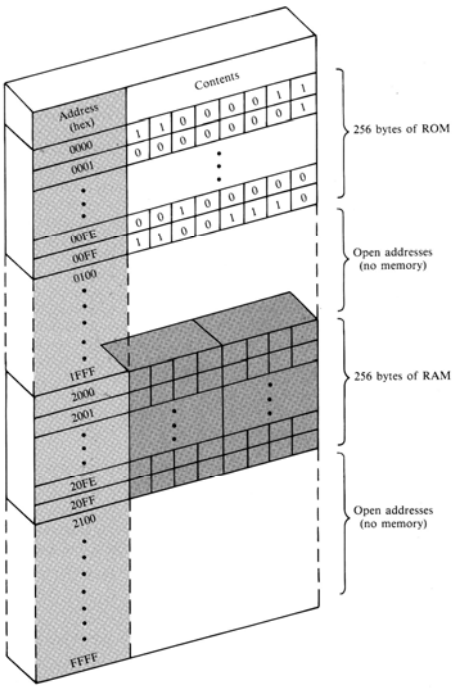

Simplified memory map showing ROM and RAM locations

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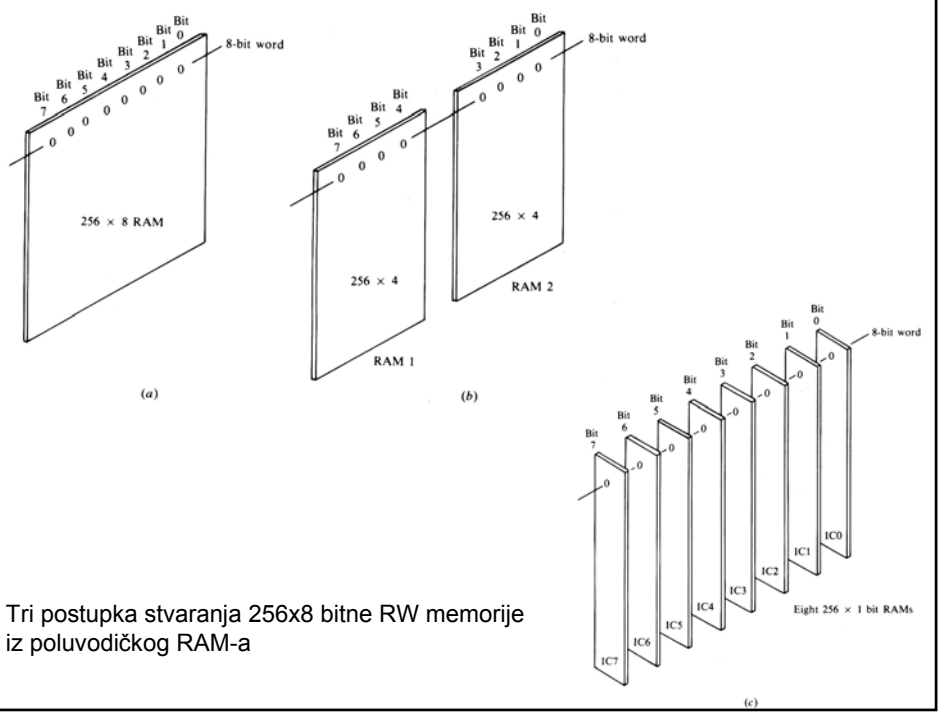
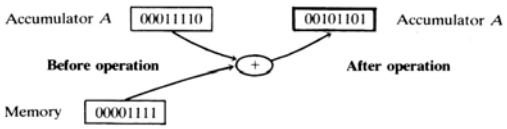


Tri postupka stvaranja 256x8 bitne RW memorije iz poluvodičkog RAM-a

Instrukcije zbrajanja i oduzimanja

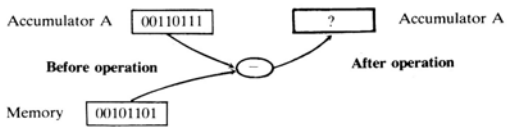
Operation	Mnemonic	Op code (hex)	Symbolic (all register labels refer to contents)
Add	ADD *A*	8B	$A + M \rightarrow A$

(*a*) Summary of the add instruction

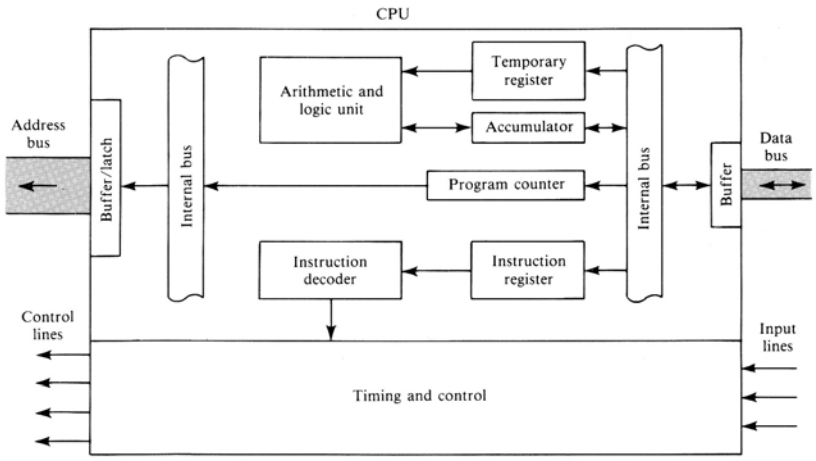


Operation	?	? (hex)	Symbolic (all register labels refer to contents)
Subtract	SUB *A*	80	$A - M \rightarrow A$

(*a*) Summary of the subtract instruction



(*b*) A subtraction problem



Simplified CPU architecture

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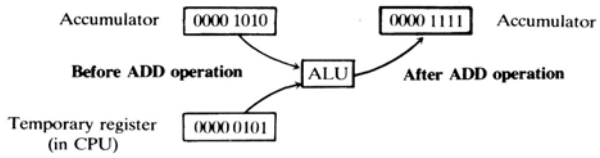
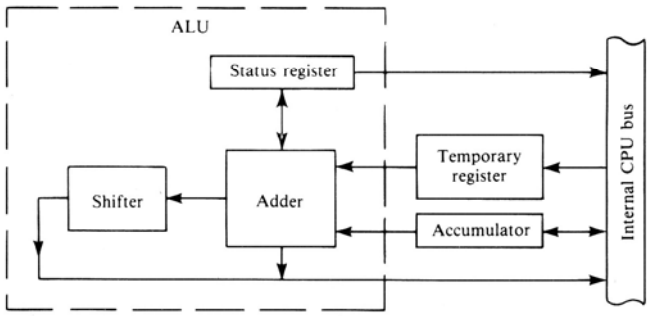


(*a*) The ALU executing the add instruction



(*b*) Organization of the ALU

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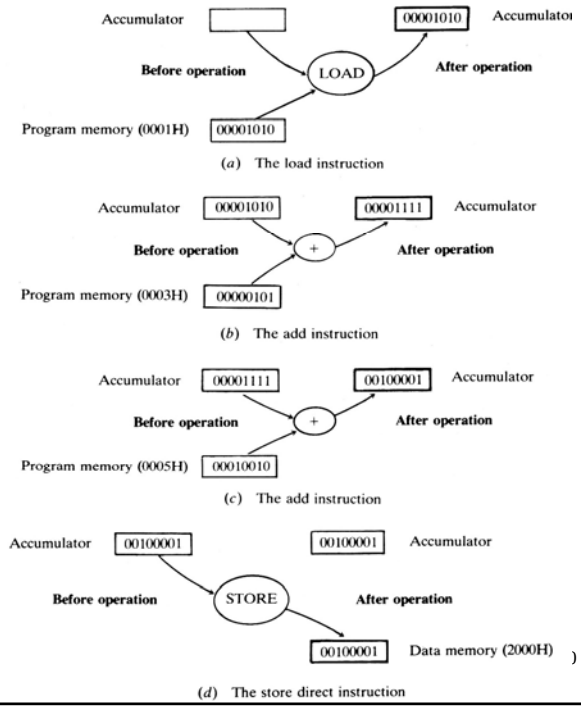
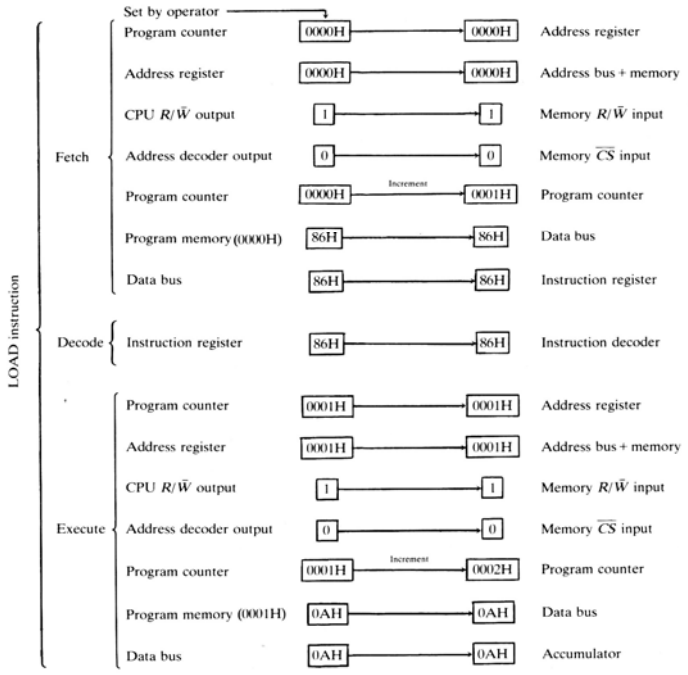
Sadržaj lokacija memorije pri zbrajanju 10 + 5 + 18

A microcomputer program segment for adding 10 + 5 + 18

Primjeri instrukcija



Analiza load instrukcije



A detailed analysis of the load immediate instruction

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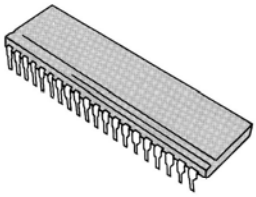
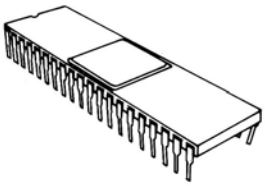
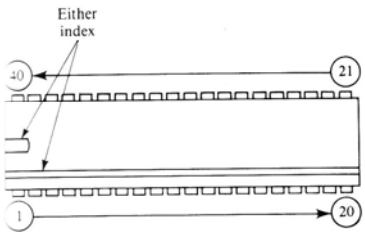
MIKROPROCESOR



(a) Plastic 40-pin DIP microprocessor

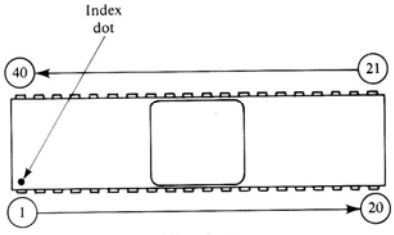


(b) Ceramic 40-pin DIP microprocessor



(Top view)

(c) Pin numbering on plastic 40-pin DIP IC



(Top view)

(d) Pin numbering on ceramic 40-pin DIP IC

Opis čipa mikroprocesora

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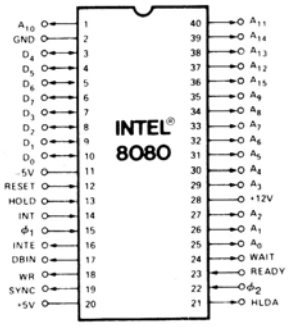
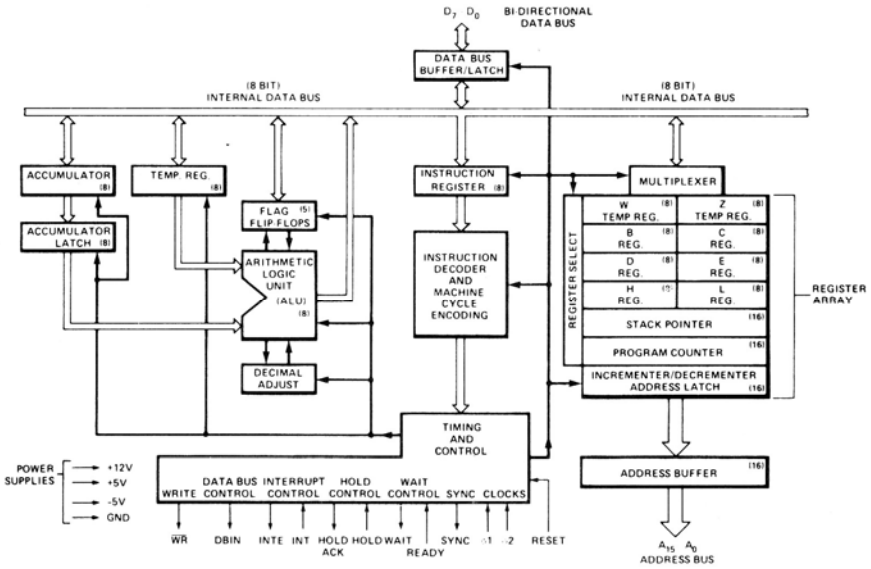
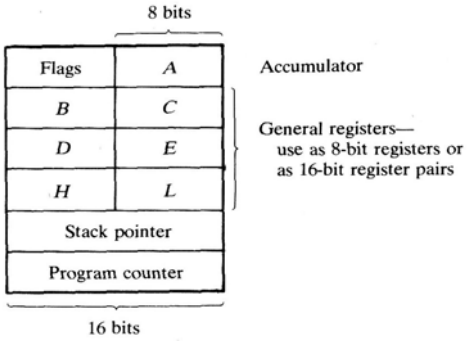


Pin name	Purpose	Input or output
GND, +5 V, −5 V, +12 V	Power supply connections	Inputs
$\phi 1$, $\phi 2$	Clock signals	Inputs
D_0–D_7	Data lines	Bidirectional
A_0–A_{15}	Address lines	Outputs
SYNC	Synchronizer	Output
DBIN	Data input strobe	Output
WAIT	MPU in wait state	Output
$\overline{WR}$	Write strobe	Output
HLDA	Hold acknowledge	Output
INTE	Interrupt acknowledge	Output
READY	Data input stable	Input
HOLD	Hold request	Input
INT	Interrupt request	Input
RESET	Reset MPU	Input

Raspored i funkcija nožica (pinova) mikroprocesora Intel 8080



(*a*) Functional block diagram of the Intel 8080 microprocessor (*Courtesy of Intel Corporation*)



(*b*) Programming registers in the Intel 8080 CPU

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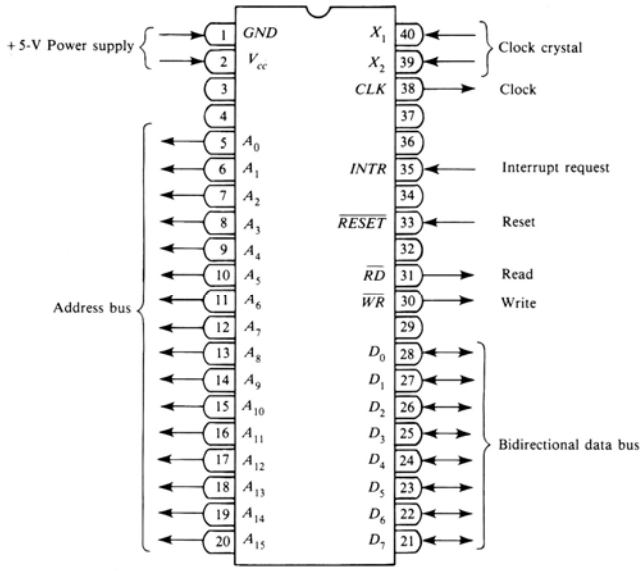

Pinovi općenitog (generičkog) procesora

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Pin name	Purpose	Input or output
GND, V_{cc}	Power supply connections	Inputs
X_1, X_2	Crystal connections for internal clock	Inputs
CLK	Clock signal	Output
A_0–A_{15}	Address bus	Outputs
D_0–D_7	Data bus	Bidirectional
$\overline{RD}$	Read control	Output
$\overline{WR}$	Write control	Output
INTR	Interrupt request	Input
$\overline{RESET}$	Reset program counter	Input

Pinovi općenitog (generičkog) procesora

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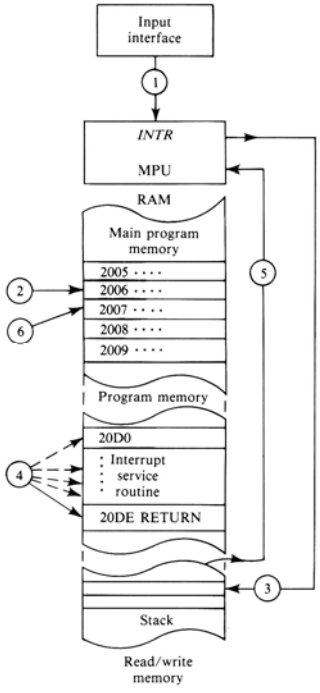
Koraci obrade prekida
na generičkom procesoru



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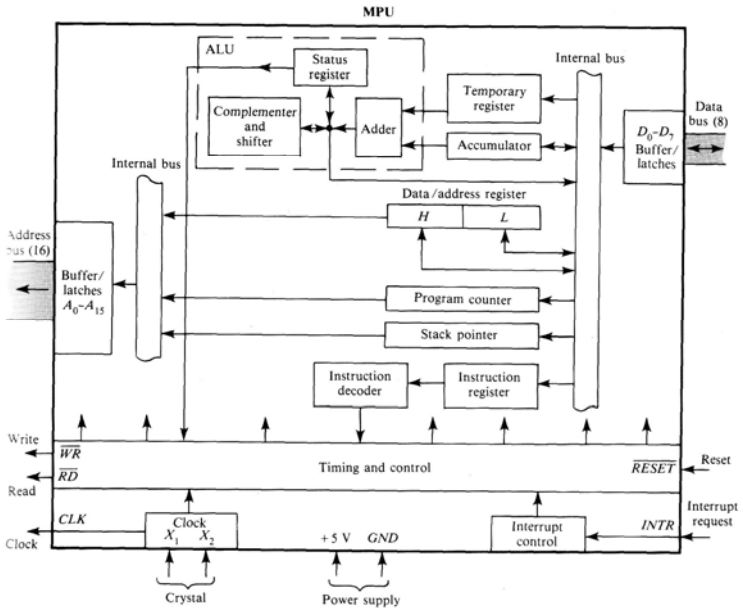
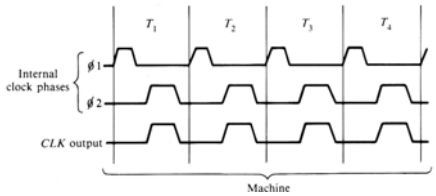
GRAĐA MIKROPROCESORA



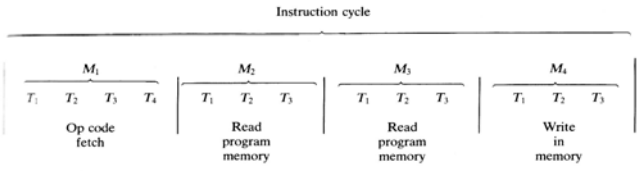
Functional block diagram of the generic microprocessor

Valni oblik signala vremenskog vođenja (clock)



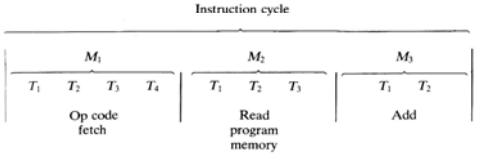
Vremenski i strojni ciklusi instrukcije spremanja i zbrajanja

STORE instruction
Store contents of accumulator in memory location given by the next two bytes in program memory



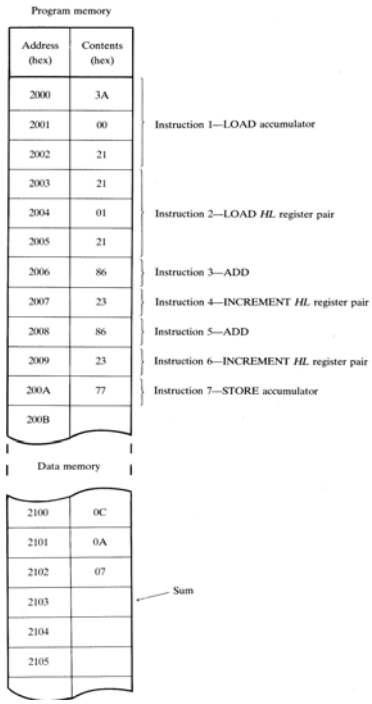
(*a*) Timing and machine cycles for a store immediate instruction

ADD instruction
Add contents of accumulator to contents of next byte in program memory and leave sum in accumulator



(*b*) Timing and machine cycles for an add immediate instruction

Sadržaj memorije i instrukcije zbrajanja



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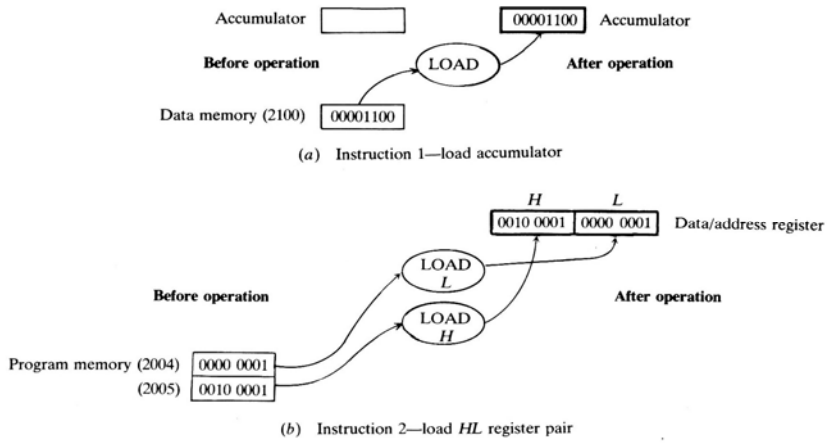
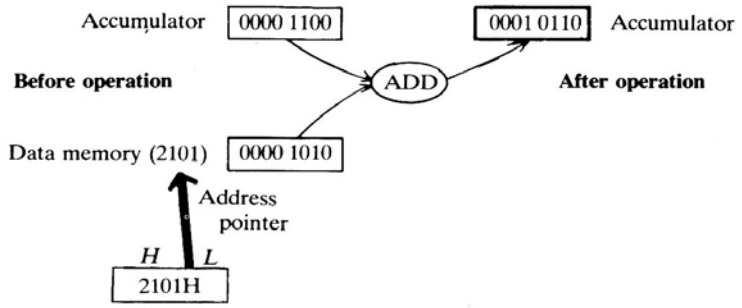
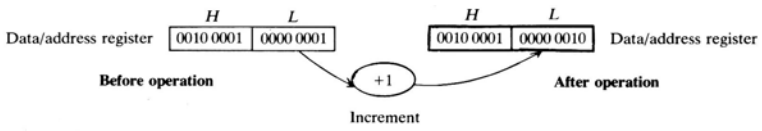


Sadržaji registara pri izvođenju instrukcija za rad s podacima i adresiranje

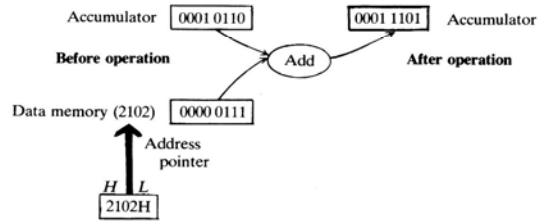


(c) Instruction 3—add

Sadržaji registara pri izvođenju instrukcija za rad s podacima i adresiranje

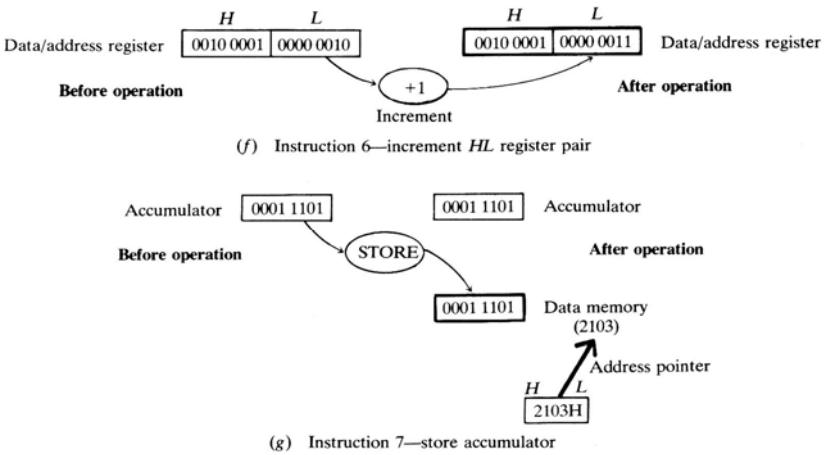


(d) Instruction 4—increment *HL* register pair



(e) Instruction 5—add

Sadržaji registara pri izvođenju instrukcija za rad s podacima i adresiranje



(f) Instruction 6—increment *HL* register pair

(g) Instruction 7—store accumulator

Sadržaji registara pri izvođenju instrukcija za rad s podacima i adresiranje

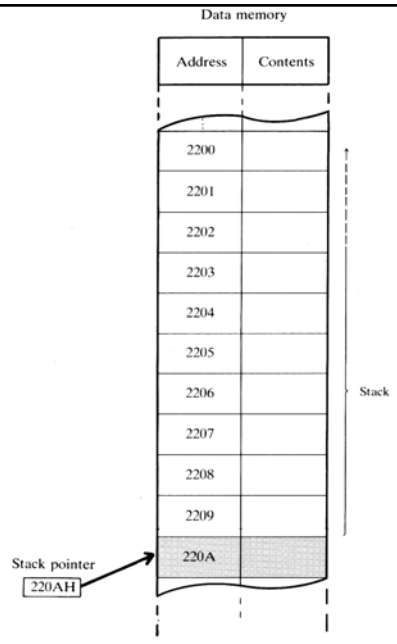


Fig. 5-15 Setting up the stack in RAM

Rad sa stogom

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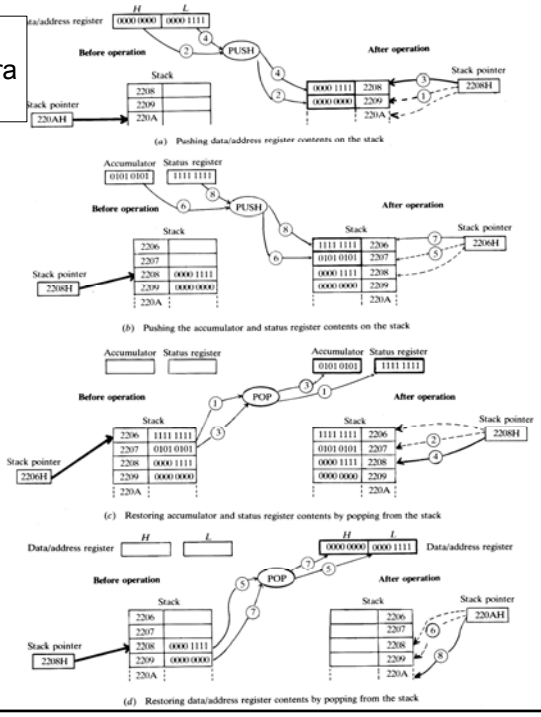
Rad sa stogom
- obnavljanje sadržaja registra vraćanjem sa stoga (POP)



PROGRAMIRANJE MIKROPROCESORA

Program memory

Address (hex)	Contents (binary)	
2000	00111110	← Start of program
2001	10110100	
2002	00101111	
2003	00110010	
2004	00000000	
2005	00100001	
2006	01110110	
2007	·	← End of program
·	·	
·	·	

(a) Binary machine code program

Program memory

Address (hex)	Contents (hex)	
2000	3E	← Start of program
2001	B4	
2002	2F	
2003	32	
2004	00	
2005	21	
2006	76	
2007	·	← End of program
·	·	
·	·	

(b) Hexadecimal machine code program

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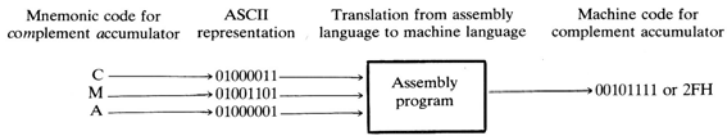
BIN i HEX oblik strojnog koda programa



(*a*) Translation of assembly language mnemonic to machine code by an assembly program

Label	Mnemonic	Operand	Comments
	MVI	*A*, B4H	; Load accumulator with the data that immediately follows, which is B4H
	CMA		; Complement the contents of the accumulator
	STA	2100H	; Store the contents of the accumulator in memory location 2100H
	HLT		; Stop MPU

(*b*) Assembly language program

Program u simboličkom strojnom jeziku

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Address (hex)	Contents (hex)	Label	Mnemonic	Operand	Comments
2000	3E		MVI	*A*,B4H	; Load accumulator with the data that immediately follows, which is B4
2001	B4				
2002	2F		CMA		; Complement the contents of the accumulator
2003	32		STA	2100H	; Store the contents of the accumulator in memory location 2100H
2004	00				
2005	21				
2006	76		HLT		; Stop MPU

(*c*) Combined machine and assembly language program

Kombinirani strojni i simbolički oblik programa

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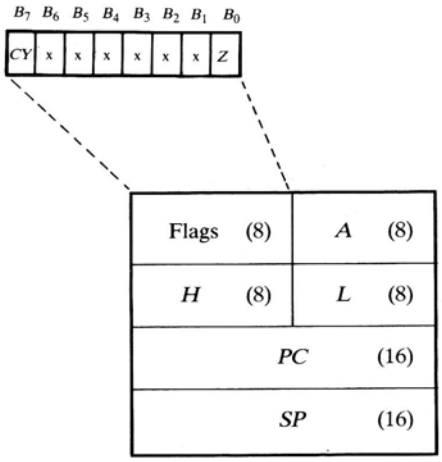
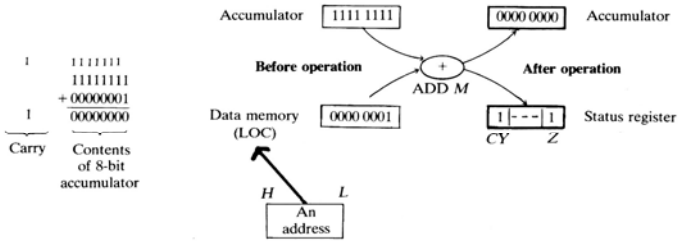
POJEDNOSTAVLJENI INSTRUKCIJSKI SKUP

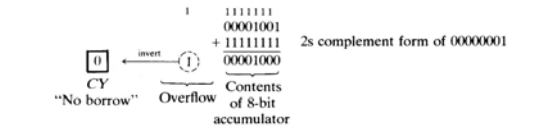


Programming model for the generic microprocessor

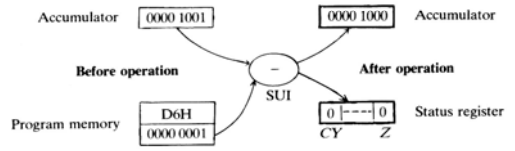


Adding binary numbers showing carry (b) The ADD M instruction's effect on the flags and accumulator

Aritmetičke instrukcije

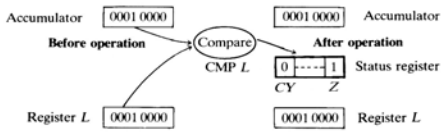


(a) Binary subtraction by converting subtrahend to 2s complement form and adding

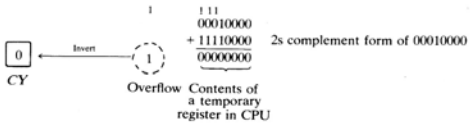


(b) The subtract immediate instruction

Aritmetičke instrukcije

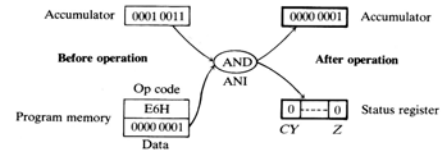


(a) The compare A with L instruction

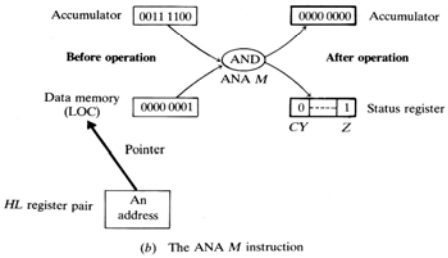


(b) Effect on carry flag when the internal CPU binary subtraction occurs during the compare operation

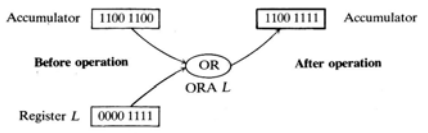
Logičke instrukcije



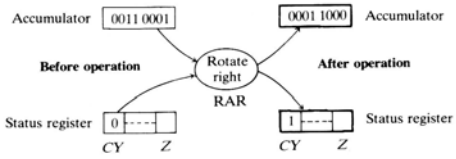
(a) The AND immediate instruction



(b) The ANA M instruction

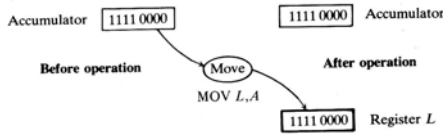


The OR A with L instruction

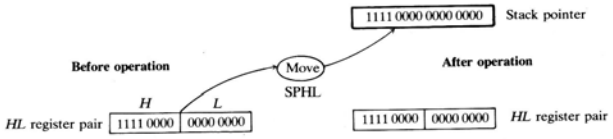


The rotate A right through carry instruction

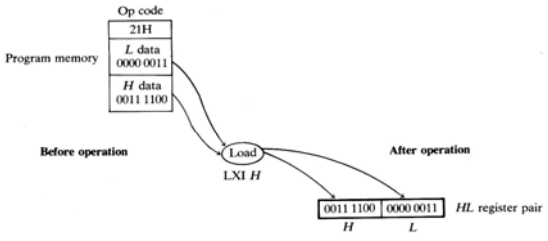
Instrukcije za prijenos podataka



The move A to L instruction



The move HL to SP instruction



The load HL immediate instruction

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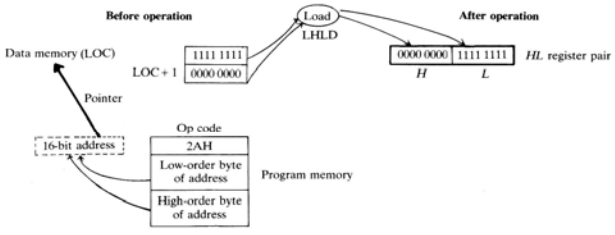
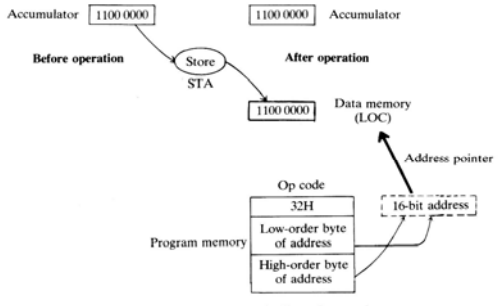
Instrukcije za prijenos podataka



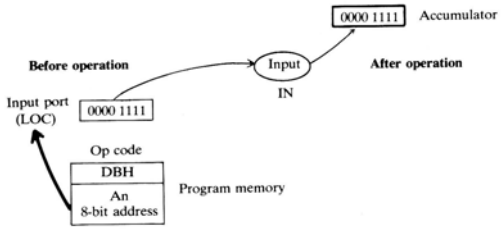
The load HL direct instruction



The store A direct instruction

36

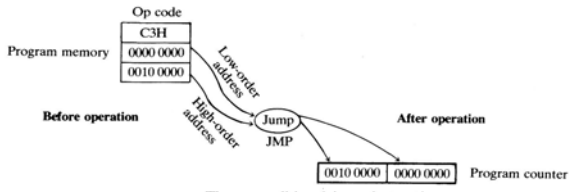
Instrukcije za prijenos podataka (sa ulaza)



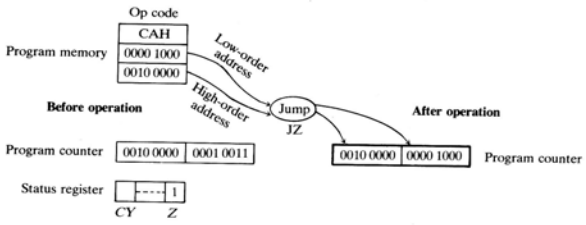
The input direct instruction

37

Instrukcije za grananje i skok u programu



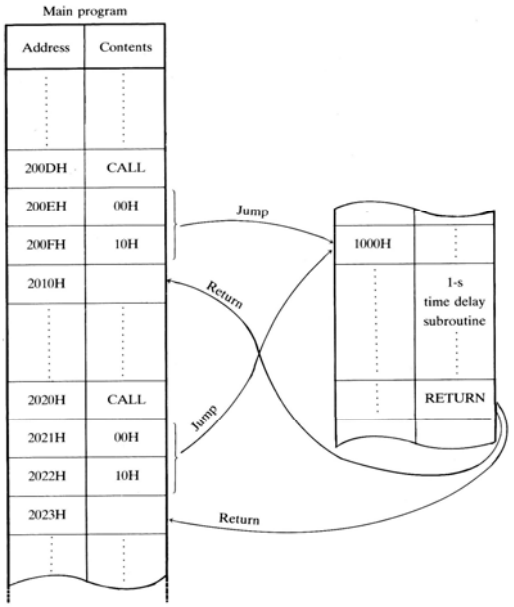
The unconditional jump instruction



The jump if zero instruction

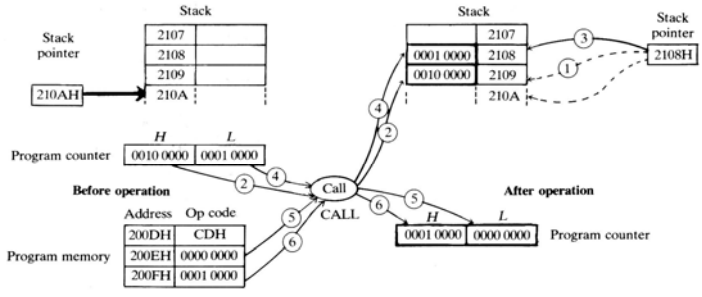
38

Instrukcije za poziv i povratak iz potprograma

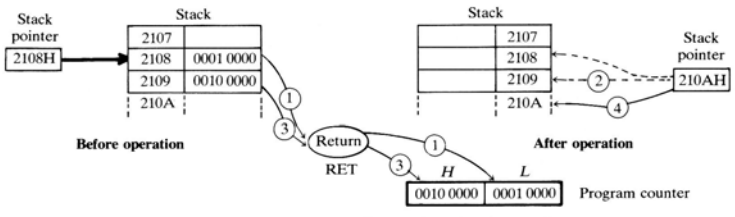


Program flow from main program to subroutine and back using call and return instructions

Instrukcije za poziv i povratak iz potprograma

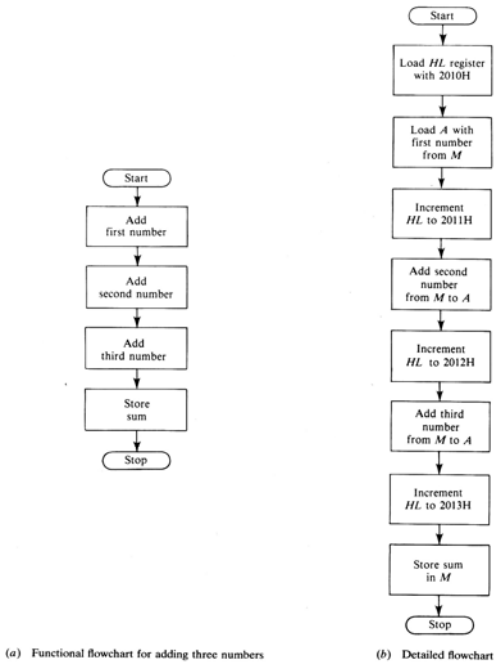


The subroutine call instruction



The return from subroutine instruction

PISANJE PROGRAMA



(a) Functional flowchart for adding three numbers (b) Detailed flowchart

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Sadržaj memorije i instrukcije za zbrajanje tri broja i spremanje zbroja

Data memory

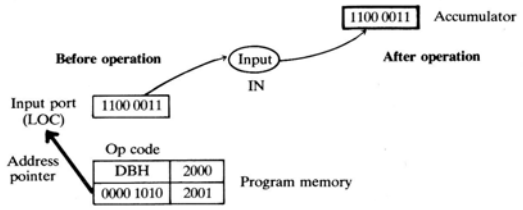
Address (hex)	Contents (hex)	
2010	0F	
2011	09	
2012	06	
2013		←Sum

Program memory

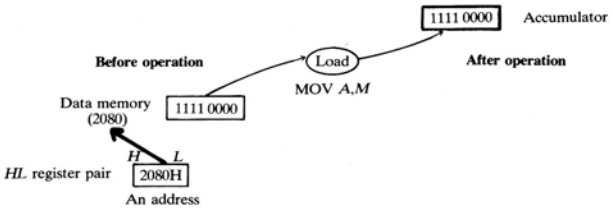
2020	21	Instruction 1—Load *HL*
2021	10	
2022	20	
2023	7E	Instruction 2—Load *A* with first number
2024	23	Instruction 3—Increment *HL*
2025	86	Instruction 4—Add second number
2026	23	Instruction 5—Increment *HL*
2027	86	Instruction 6—Add third number
2028	23	Instruction 7—Increment *HL*
2029	77	Instruction 8—Store sum
202A	76	Instruction 9—Stop

Memory contents and instructions for adding three numbers and storing the sum

NAČINI ADRESIRANJA



The input instruction (direct addressing)



The load *A* from memory instruction (register indirect addressing)

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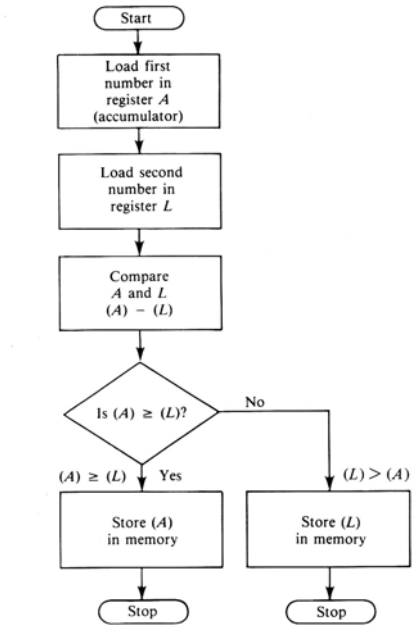
GRANANJE PROGRAMA



(*a*) Detailed flowchart for comparing and storing the larger number

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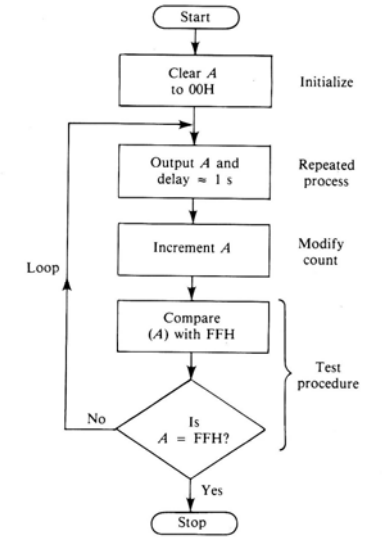
PONAVLJANJE DIJELOVA PROGRAMA (PETLJE)



Flowchart of the counting problem that uses program loopin

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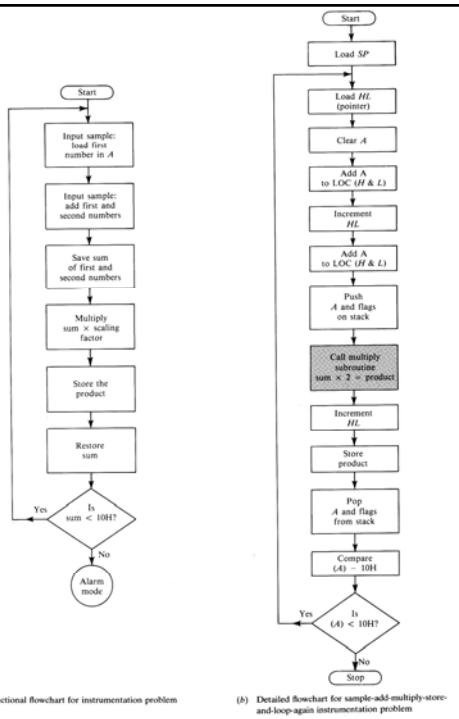
POTPROGRAMI



(a) Functional flowchart for instrumentation problem

(b) Detailed flowchart for sample-add-multiply-store-and-loop-again instrumentation problem

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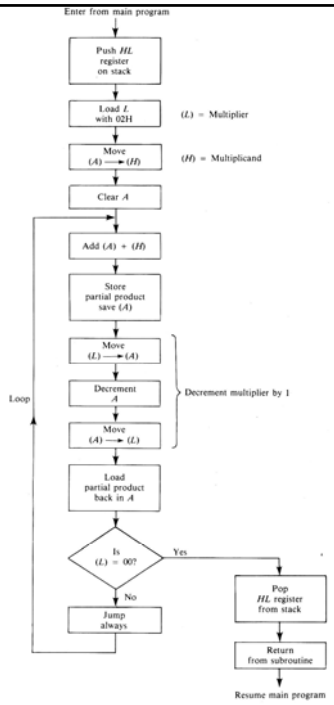
POTPROGRAMI



Detailed flowchart of multiply subroutine used in instrumentation problem

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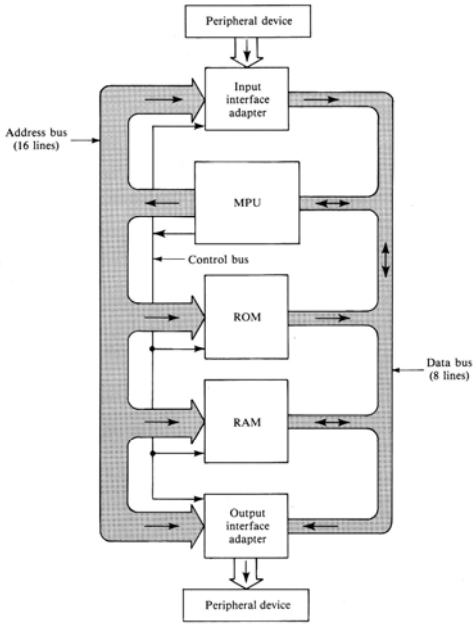
SPAJANJE MIKROPROCESORA NA VANJSKE JEDINICE



Block diagram of microprocessor-based system

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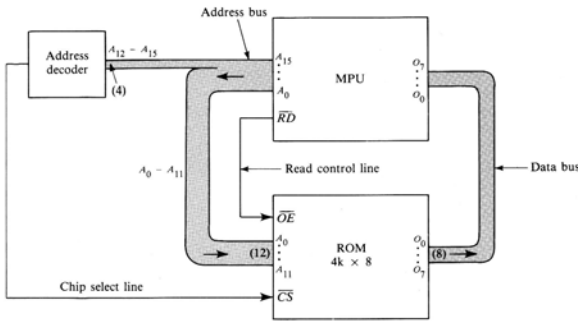
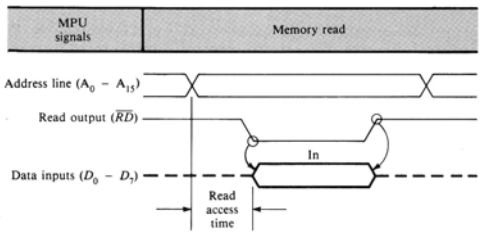
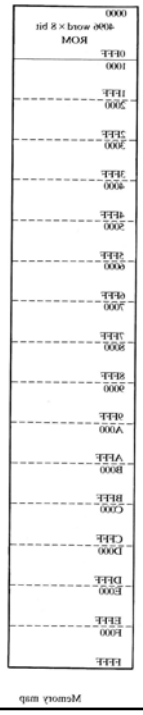
Sučeljavanje prema ROM-u



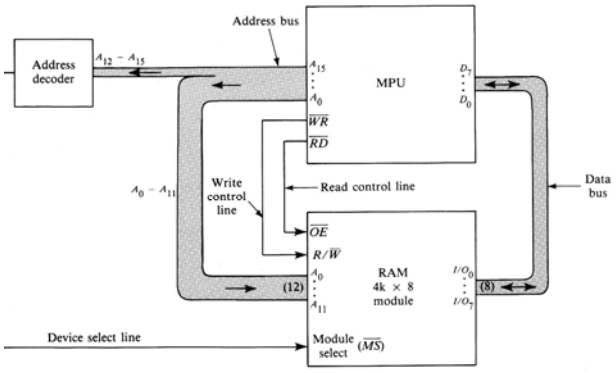
Interfacing ROM with microprocessor



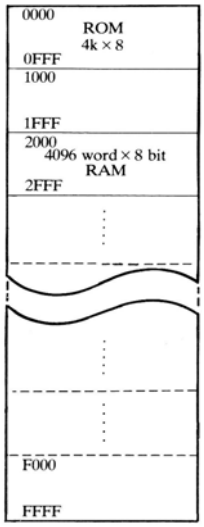
Timing diagram—MPU signals during ROM read operation



Sučeljavanje prema RAM-u



Interfacing RAM with microprocessor



Memory map

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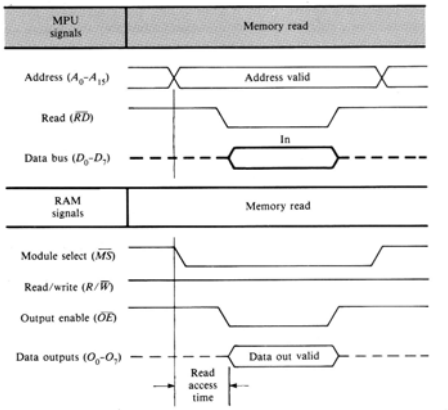
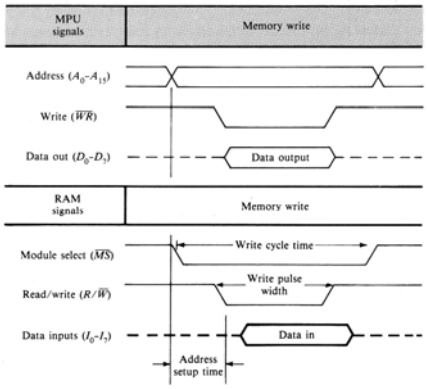
Sučeljavanje prema RAM-u



Timing diagram—MPU and RAM signals during memory read operation



Timing diagram—MPU and RAM signals during memory write operation

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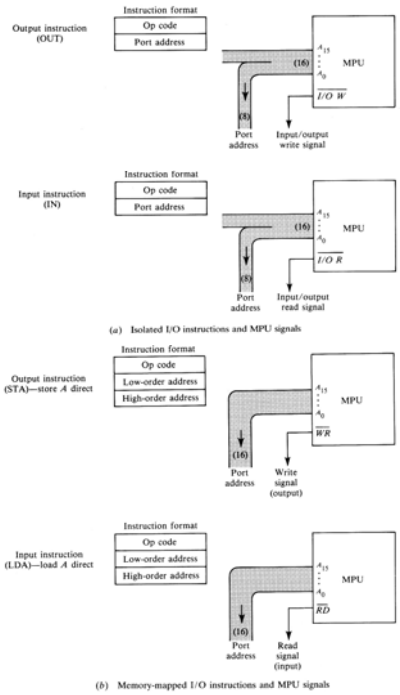
Sučeljavanje prema ulazu/izlazu



(a) Isolated I/O instructions and MPU signals

(b) Memory-mapped I/O instructions and MPU signals

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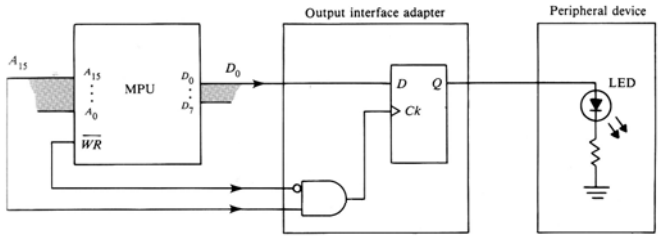
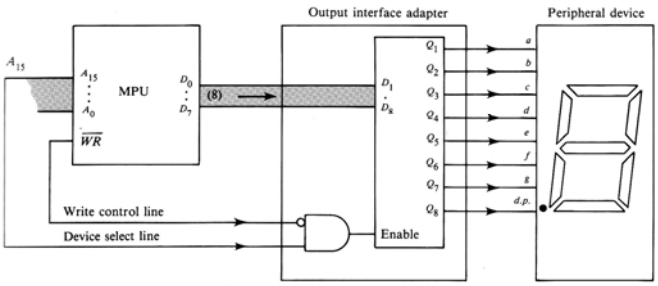
Sučeljavanje prema 7-segmentnom pokazivaču



(a) Interfacing single LED output bit indicator



(b) Interfacing seven-segment display

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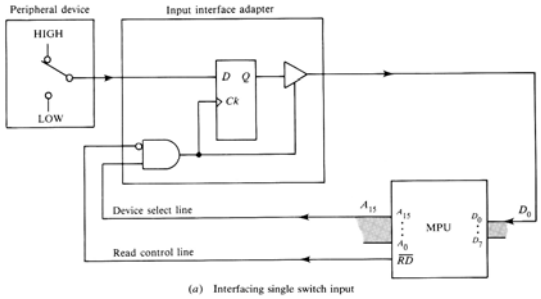
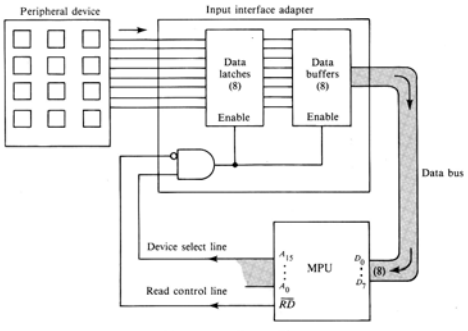
Sučeljavanje prema tipkovnici



(a) Interfacing single switch input



(b) Interfacing keyboard input

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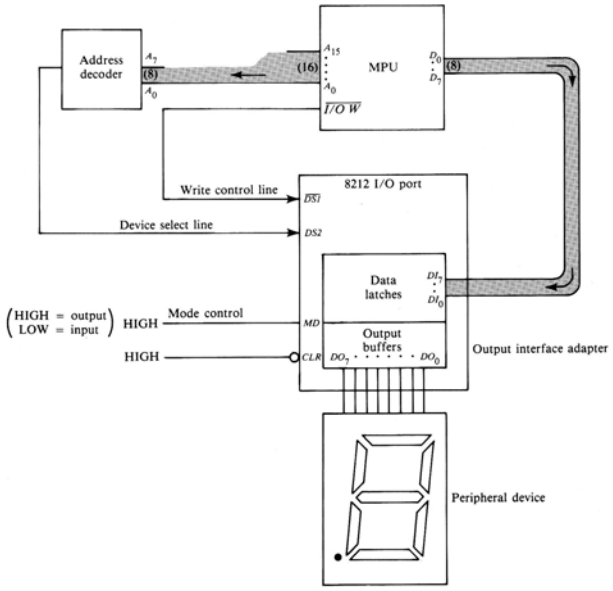
Sučeljavanje prema ulazno/izlaznim pristupima



Interfacing with seven-segment display using Intel 8212 I/O port

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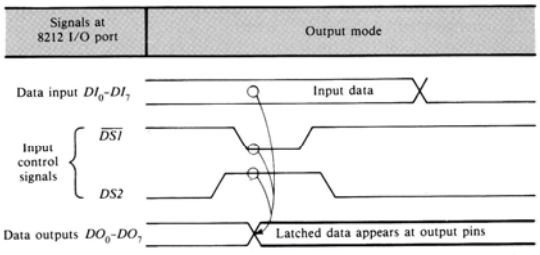
Sučeljavanje prema ulazno/izlaznim pristupima



Timing diagram—I/O port signals during output mode

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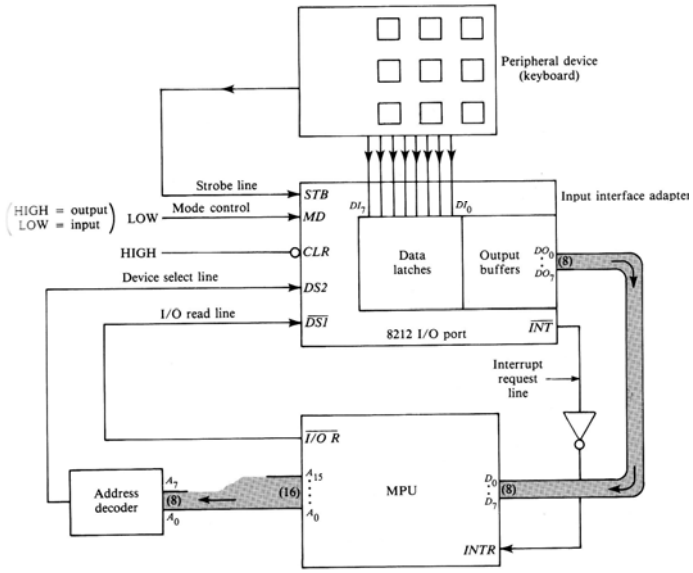
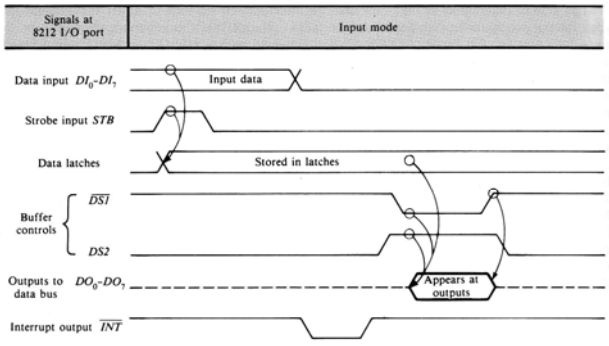
Sinkronizacija U/I prijenosa podataka prekidima



Interfacing with keyboard using the Intel 8212 I/O port with simple interrupt

57

Sinkronizacija U/I prijenosa podataka prekidima



Timing diagram—I/O port signals during input mode with simple interrupt

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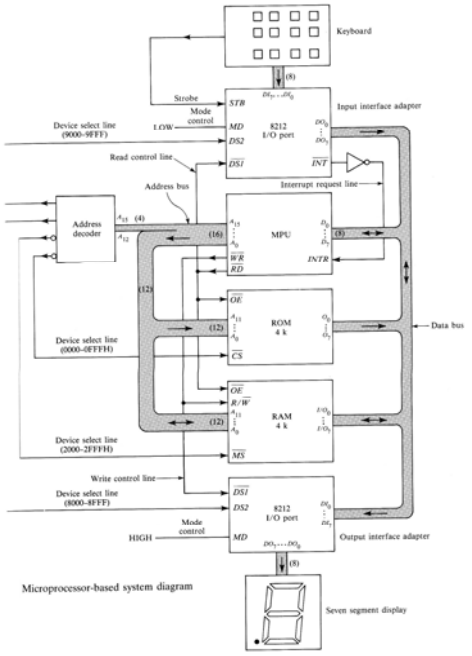
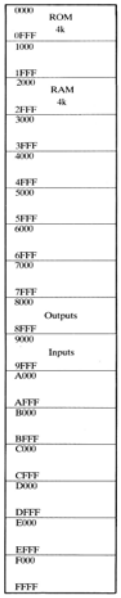
Dekodiranje adresa



Microprocessor-based system diagram



Memory map for microprocessor-based system

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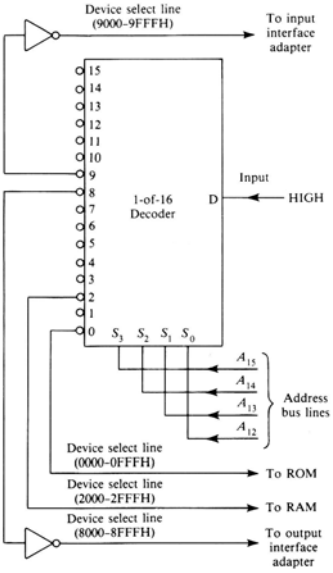
Dekodiranje adresa



Using the 1-of-16 decoder as an address decoder

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Dekodiranje adresa